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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,796	07/10/2003	Timothy P. Gibson	H0004400	1971

128 7590 02/05/2008

HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
02/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/616,796	GIBSON ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-16,18-24 and 26-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-16,18-24 and 26-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments (1/9/2008) with respect to the rejection of claims 1-9, 11-16, 18-19, 21-24, 26-54, 57-59 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 18, 34, 60 are objected to because of the following informalities:

Claim 18, recites: "and simultaneously generate more than one output signal", should be corrected to "signals"; also (end of third paragraph): "; said_digital processing..." the "_" should be removed.

Claim 34, recites: "...receiving at a plurality the one or more front-end circuits..."

Claim 60, recites: "...and simultaneously generate more than one output signal..." should be corrected to "signals".

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-9, 11-16, 46-52 of instant application (10/616796) are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 10/563397 in view of Kaminski et. al., (U.S. 6,678,512).

With respect to claim 1 of the instant application, all of the limitations of claim 1 are disclosed in claim 1 of co-pending case 10/563397, except for the limitations "simultaneously carrying a plurality of channels within said frequency band" and "...digital signal simultaneously carrying said plurality of channels within said frequency band...". Instead claim 1 of copending application recites: "corresponding to a plurality of channels within said frequency band...". In the same field of endeavor, Kaminski et. al., disclose: "simultaneously carrying a plurality of channels in a frequency band " and "...digital signal simultaneously carrying said plurality of channels within said frequency band..." (column 5, lines 40-48, where channels in the frequency range are simultaneously received by the antenna that receiving signals in the same frequency range, and column 6, lines 6-8, 18-20) the digital signal simultaneously carrying said plurality of channels within said frequency band...") At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify claim 1 of 10/563397

based on the teachings of Kaminski et. al., so that the analog signal simultaneously caries a plurality of channels in a frequency band, and a digital signal is generated simultaneously carrying said plurality of channels in the frequency band, to allow processing of signals in RF frequency bands that include plurality of channels in the nyquist zone of the A/D converter (column 3, lines 24-30).

Claims 2-9, 11, 15-16 of instant application are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2-9, 10-11, 12-16 of co-pending application 10/563397

With respect to claim 46 of instant application, claim 46 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 10,17 (of co-pending case 10/563397) based on a rationale similar to the one used above in the nonstatutory obviousness-type double patenting rejection of claim 1. Furthermore, claim 46 recites: " wherein said frequency band comprises aviation-band radio signals..."not disclosed by claims 1,10 of 10/563397. However, frequency bands with aviation-band signals, are known in the art and it would have been obvious to a person of ordinary skill in the art to modify claims 1,10 of 10/563397 so that the mentioned frequency band is a frequency band aviation-band signals, so that the particular type of signals, aviation-band signals are processed.

With respect to claim 52, see claim 4 of 10/563397.

Claims 47-49 recite specific aviation-band signals, and would have been obvious to a person of ordinary skill in the art to modify claims 1, 10 so that specific aviation signals are received.

Claims 50-51, see claims 2-3 of 10/563397.

Claims 18-24, 26-28, 29-33, 53-54 of instant application (10/616796) are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 18-28 of copending Application No. 10/563397 in view of Kaminski et. al., (U.S. 6,678,512).

With respect to claim 18 of instant application, claim 18 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 18,19,20, 25, (of co-pending case 10/563397) based on a rationale similar to the one used above in the nonstatutory obviousness-type double patenting rejection of claim 1.

Claims 19, 21-24, 26-28 instant application are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 19, 21-24, 26-28 respectively.

Claim 29 is rejected similarly to claim 18 above, on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 18,19,20, 25, (of co-pending case 10/563397),with respect to the plurality of front-end circuits, and plurality of analog to digital converters (of claim 29), it would have been obvious to a person of ordinary skill in the art to modify claims 18,18,20,25 (of co-pending case 10/563397), to have a plurality of front-end circuits, and plurality of analog to digital

converters, (instead of at least one of these components) to perform parallel (faster) processing functions using plurality of the aforementioned components

Claims 30-33, see claims 22-24 of 10/563397.

Claim 53 is rejected similarly to claim 18 above, on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 18,19,20, 25, (of co-pending case 10/563397), with respect to the radio signals comprising aviation navigation and aviation communication radio signals, as specified in claim 53, such signals are known in the art ,and it would have been obvious to a person of ordinary skill in the art to modify claims 18,19,20, 25, (of co-pending case 10/563397) , so that aviation related signals are received and processed.

Claim 54, see claim 19 of 10/563397.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lehman et. al., (U.S. 6,282,184).

With respect to claims 1, 5-9, Lehman et. al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band (Fig. 2, front-end comprises antenna 3, and wideband receiver 40, column 2, lines 60-67, column 3, line 1, (also column 6, lines 56-66) see reception of composite RF signal containing RF signals associated with a respective standard, see also Fig. 3 (showing details of Fig. 4), frequency band is a 15MHz band, see column 31-47) and generate an analog signal simultaneously carrying a plurality of channels within said frequency band (see Fig. 3, output of BPF filter 51, a multichannel signal, see column 8, lines 11-15); an analog to digital converter coupled to said front-end circuit (Fig. 3, A/D converter 41), said analog to digital converter operable to convert said analog signal to a digital signal simultaneously carrying said plurality of channels within said frequency band (column 8, lines 13-18); and a digital processing system coupled to said analog to digital converter, said digital processing system operable to receive said digital signal (Fig. 2, see digital processing system comprising blocks 7-9 (channelizers) and 13-15 DSPs) and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (column 4, lines 6-15, separation/processing of channel of the particular protocol).

With respect to claim 4, Lehman et. al., further disclose: wherein said digital processing system generates a plurality of output signals comprising a plurality of signals for transmission to a plurality of end devices (Fig. 2, see plurality of N streams

generated by DSPs and they're supplied to PSTN network, (comprising a plurality of phones as end devices)).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 5-8, 11-16, 34-36, 38, 43 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kaminski et. al., (U.S. 6,678,512).

With respect to claim 1, Kaminski et. al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal simultaneously carrying a plurality of channels within said frequency band (Fig. 3, see antenna 12a, filter 20a, amplifier 52a, frequency band 824-849MHz, see column 5, lines 40-47, see the frequency channels (simultaneously carried) within specified frequency range, received by front-end, column 5, lines 51-56); an analog to digital converter coupled to said front-end circuit (Fig. 3, A/D block 24), said analog to digital converter operable to convert said analog signal to a digital signal simultaneously carrying said plurality of channels within said frequency band (column 5, lines 62-65, column 6, lines 17-21, where the A/D receives the signals (channels) in cellular band

and PCS band (see combiner shown in Fig. 3) and converts these to digital); and a digital processing system coupled to said analog to digital converter (Fig. 3, block 26, DSP), said digital processing system operable to receive said digital signal and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (column 4, lines 66-67 , column 5, lines 1-10, DSP retrieves digital signals (this corresponds to generating at least one output signal corresponding to at least one of said plurality of channels with said frequency band) by performing digital signal processing (and generates at least one output signal see Fig. 3 arrow out of DSP block)) .

With respect to claim 5, Kaminski et. al., disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (Fig. 3, see antenna 12a).

With respect to claim 6, Kaminski et. al., disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (Fig. 3, LNA, block 52a).

With respect to claims 7, 8 Kaminski et. al., disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (Fig. 3, filter 20a, bandpass filter , column 5, lines 54-56).

With respect to claim 11, Kaminski et. al., further discloses: wherein said digital processing signal further comprises a digital down converter operable to select said at least one of channels within said frequency band (column 5, lines 1-10, where tuning to respective frequencies within the DSP corresponds to the function of the claimed downconverter); wherein said digital down converter selects at least one of said channels according to configurable channel selection parameters (see column 7, lines 57-64, software programmable receiver, and column 5, lines 1-8,where digital detection, decimation, tuning are configurable channel selection parameters).

With respect to claims 12-16 see above rejection of claim 11 (where the channel decoding parameters, see use of digital detectors and channel selection , column 5, lines 1-8).

With respect to claim 34, Kaminski et. al., disclose: providing a radio receiver comprising: one or more front-end circuits (Fig. 3, see at least two front-end circuits each comprising antenna, filter and LNA); one or more analog to digital converters coupled to said one or more front-end circuits (Fig.3, A/D 24, coupled to front-end circuit); and a digital processing system coupled to said one or more analog to digital converters (Fig. 3, DSP), said digital processing system comprising :a digital down converter (part of DSP and therefore coupled to it, see column 4, lines 66-67, column 5, lines 1-9); and a digital signal processor coupled to said digital down converter (DSP mentioned above, the tuning to respective frequencies); receiving at a plurality the one

or more front-end circuits a plurality of radio signals transmitted across a frequency band (Fig. 3, see signals to combiner 56, the plurality of signals within cellular and PCS bands, column 5, lines 40-51, 63-67) , wherein said radio signals received by any one of said front-end circuits are within a different frequency band than said radio signals received by the other of said front-end circuits (Fig. 3, see different frequency bands, cellular band and PCS band); generating an analog signal from said received radio signals, said analog signal simultaneously carrying a plurality of channels within said frequency band (column 5, lines 62-65); converting said analog signal to a digital signal simultaneously carrying said plurality of channels within said frequency band to thereby digitize said plurality of channels within said frequency band (Fig. 3, A/D converter 24, column 6, lines 18-25); and generating at least one output signal corresponding to at least one of said digitized channels within said frequency band (Fig. 3, DSP block 26. column 4, lines 66-67, column 5, lines 1-9, see retrieval and processing of digital signals (the replica cellular and PCM bands)).

With respect to claims 35-36, 38 see above rejection of claims 6-7 and 11-15 respectively.

With respect to claim 43, see above rejection of claim 34.

9. Claims 2-3, 39-42, 44-45, 46-52, 53-54, 57, 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminski et. al., (U.S. 6,678,512) in view of Phillips et. al., (U.S. 5,859,878).

With respect to claims 2,3, the limitations of these claims are not expressly taught by Kamiski et. al., In the same field of endeavor, wireless communications, Phillips et. al., disclose: wherein said digital processing system generates a single output signal comprising a time-domain multiplexed serial data link multiplexed serial data link (see Fig. 8B, (coupled to the system of 8A) where a serial interface is used to supply signals to the computer, see column 7, lines 47-52, and see Fig. 6, shows TDM processing at the receiver, that results into TDM outputs). ; further comprising a controller coupled to said digital processing system, said controller operable to receive said time-domain multiplexed serial data link and generate a plurality of signals to a plurality of end devices (Fig. 12B, line transceiver and system bus, supplying serial data to plurality of end devices in computer, column 16, lines 14-17, uart (serial communication) , and see column 15, lines 50-56).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski et. al., based on the teachings of Phillips et. al., to achieve high-speed transfer of data (TDM serial data) and supply data to a plurality of external users (intercom).

With respect to claims 39-40, 41-42 see above rejection of claims 2-3 (time-domain multiplexed signals correspond to a plurality of output signals).

With respect to claims 44-45 see above rejection of claims 2-3 above.

With respect to claim 46 see above rejection of claim of claim 43, with respect to the limitation not taught by Kaminski et al.,:aviation band radio signals; this limitation is disclosed by Phillips et. al., (in the field of wireless communications)(see column 1 through column 2, table 1 signals in aviation band, see also column 2, liens 45-56). At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski et. al., so that it functions in a frequency band (that) comprises aviation band radio signals, in order to process aviation band signals in the nyquist bandwidth without requiring frequency conversion stages to down convert analog RF signals, column 3, lines 20-30).

With respect to claims 47-49, 50-51, 52 see above rejection of claims 46, and 2-3.

With respect to claims 53-54 these claims are rejected based on a rationale similar to the one used to reject claims 49, 52.

Wit respect to claims 57, 59 these claims are rejected based on a rationale similar to the one used to reject claims 53 and 38 respectively.

10. Claims 60, 18-23, 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminski et. al., (U.S. 6,678,512) in view of Analog Devices AD6624A data sheet 2002 (hereinafter referred to as the Analog Devices document)

With respect to claim 60, Kaminski et. al., do not expressly teach: wherein said digital processing system is operable to receive said digital signal and simultaneously generate more than one out signals corresponding to more than one of said plurality of channels within said frequency band.

In the same field of endeavor, the Analog Devices document discloses: digital processing system is operable to receive said digital signal and simultaneously generate more than one out signals corresponding to more than one of said plurality of channels within said frequency band (page 14, input data ports section on left column, and schematic on front page where four tuner channels are shown see also product description section on the front page, see digitization of entire spectrum (frequency band) of carriers (channels) and selection of carriers (channels)).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski et. al., because it eliminates redundant radios in wireless applications and allows for easy reconfiguration and a variety of applications (see front page of AD6624 spec sheet).

With respect to claim 18, claim 18 see above rejection of claim 34, and claim 18 is rejected based on a rationale similar to the one used to reject claim 60 above:

With respect to claims 19, 21-23, 26-27 see above rejection of claims 18, 5-7, 11-12, 14-15,

11. Claims 1-9, 11-16, 29-33, 34-42, 43-45, 46-52, 53-54, 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et. al. (U.S. 5,859,878) in view of Caldwell et. al., (U.S.5,548 839).

With respect to claim 1, Phillips et. al. disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to said frequency band (Fig. 3A, front-end includes blocks 102 104 see column 25, lines 31-38 where the AIU receives LOC and GS analog signals from the respective antennas , column 25, lines 47-53 where a NB analog signal is generated); an analog to digital converter coupled to said front-end circuit, said analog to digital converter operable to receive and convert said analog signal to a digital signal (column 25, lines 49-52, narrowband ADC 202 see Fig. 3A (or wideband ADC when other types of signals are processed)); and a digital processing system coupled to said analog to digital converter, said digital processing system operable to receive said digital signal and generate at least one output signal within said frequency band (see Fig. 1, block 106b, also shown in Fig. 3A, see column 23, lines 5-7, 24-28), said digital processing system comprising: a digital down converter (Fig. 3A, block DDC, details shown in Fig. 8A, digital downconverter 210, column 23, lines 5-7, column 26, lines 29-31, the control words are used to frequency control the DDC); a digital signal processor

coupled to said digital down converter (Fig.3A, elements DSP 216, and DDC element 210)

Phillips et. al. do not expressly teach: an analog signal simultaneously carrying a plurality of channels within said frequency band; a digital signal simultaneously carrying said plurality of channels within said frequency band.

In the same field of endeavor, Caldwell disclose: an analog signal simultaneously carrying a plurality of channels within said frequency band (Fig. 5A, Fig. 5B, column 4, lines 44-47, analog receiver receives (analog) RF signals, see column 8, through column 9, example 1 (or any other example)), simultaneously carrying said plurality of channels within said frequency band (see column 8, lines 53-58, all signals (these are channels) in the range)).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Phillips et. al. based on the teachings of Caldwell so that the analog signals received by Phillips et., al., simultaneously carry a plurality of channels within said frequency band, so that minimal components are used for CNST functions between 2 and 2000MHz (column 4, lines 59-67, column 5, lines 1-17). Based on the combination of teachings of Phillips and Caldwell, the digital signal of Phillips signal simultaneously carries said plurality of channels within said frequency band.

With respect to claim 2, Phillips et.al., further disclose: wherein said digital processing system generates a single output signal comprising a time-domain

multiplexed serial data link (see Fig. 8B, (coupled to the system of 8A) where a serial interface is used to supply signals to the computer, see column 7, lines 47-52 , and see Fig. 6, column 23, liens 34-36 where the signal processing (ILS processing) is performed in a TDM fashion).

With respect to claims 3 and 4 all of the limitations of claims 3 and 4 are rejected above in claim 2 (the plurality of signals are generated by the UART and supplied to the plurality of components in computer 112 (the plurality end devices) as shown in Fig.8B).

With respect to claim 5, Phillips et. al., further disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (see column 25, lines 36-37 LO, MB, and GS antennas).

With respect to claim 6, Phillips et. al., further disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (column 20,lines 58-67, see signal amplification).

With respect to claim 7, Phillips et. al. further disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (column 20, lines 58-67,line 65 mentions RF filtering).

With respect to claim 8, Phillips et.al., do not expressly teach: wherein said filter circuit comprises a filter selected from the group consisting of high-pass filter, low-pass filter, band-pass filter, notch filter, and combinations thereof.

However to a person skilled in the art at the time of the invention, high-pass filter(s), low-pass filter (s), band-pass filter(s), notch filter(s), and combinations thereof, are known filtering means, therefore it would have been obvious to a person skilled in the art at the time of the invention to modify the system of Phillips et. al., to configure the filter circuit to comprise a band-pass filter since bandpass filters remove unwanted portions of the RF signal.

With respect to claim 9, Phillips et. al., further disclose: wherein said front-end circuit further comprises an intermediate frequency mixing circuit operable to translate said received radio signals to an intermediate frequency band (column 8, lines 36-38, where IF conversion involves mixing the received RF signals so that they are downconverted to IF).

With respect to claim 11, Phillips et. al., further disclose: wherein said digital processing system further comprises a digital down converter operable to select said at least one of said channels within said frequency band, wherein said digital down converter selects said at least one of said channels according to configurable channel selection parameters (see column 26, lines 29-31, 41-44, where the configurable

parameter is the frequency used for frequency tuning (during the tune period shown in Fig. 6, see column 23, lines 34-39) to select the LO, GS channels).

With respect to claim 12, Phillips et. al., further disclose: wherein said configurable channel selection parameters are software configurable (see column 22, lines 61-67, column 23, lines 1-4, and column 11, lines 49-51, where the DSP executes a RAM program to perform the ILC processing the involves using different tuning frequencies for the LO, GS signals).

With respect to claim 13, all of the limitations of claim 13 are rejected above in claim 11 (see frequency tuning i.e. the channel frequency is changed).

With respect to claim 14, Phillips further discloses: wherein said digital processing system comprises a digital signal processr, said digital signal processor operable to extract information from said at least one of said channels and generate said at least one output signal, wherein said digital signal processor extracts said information from said at least one of said selected channels according to configurable channel decoding parameters (see column 2, lines 51-56, where received waveforms of various combinations of amplitude, frequency, and phase modulations are processed, see column 10, lines 58-65, where demodulation of any combination of amplitude, frequency, and phase modulation corresponding to the channel decoding parameters, is performed by DSP 216).

With respect to claim 15, Phillips et. al. further disclose: wherein said configurable channel decoding parameters are software configurable (see column 22, lines 61-67, column 23, lines 1-4, and column 11, lines 49-51, where the DSP executes a RAM program to perform the ILC processing including demodulation/decoding).

With respect to claim 16, Phillips et. al., further disclose: wherein said configurable channel decoding parameters are selected from the group consisting of channel frequency, channel modulation scheme, channel bandwidth, channel information format, and combinations thereof (see channel modulation scheme, column 21, lines 58-665, where demodulation of any combination of amplitude, frequency, and phase modulation).

With respect to claims 29, 30-33, these claims are rejected based on a rationale similar to the one used to reject claim 1,11, 14 (for claims 29, 33) and 6-7, 9.

With respect to claims 34-42, these claims are rejected based on a rationale similar to the one used to reject claims 29-32, 4.

With respect to claim 43, Phillips discloses: a plurality of front-end circuits (Fig. 3, where the front-end circuit group is shown as block 103 "AIU" antenna interface unit (including processing prior to the analog submodule see column 20, lines 58-67) where

the AIU includes LOC, MB, GS antennas (not shown) see column 25, lines 31-41, and these antennas are tuned for the Localizer, Marker Beacon and Gliseslope signals (used for landing) that have different frequency bands) each of which is operable to receive a plurality of radio signals transmitted across a frequency band and generate analog signals that are combined into a composite analog signal corresponding within said frequency band (see column 25, lines 39-41, see addition of antenna inputs (analog singals)); a single analog to digital converter operable to receive the composite analog signal and convert the composite analog signal to a single digital signal (see column 25,lines 50-52, the NB ADC is used); a digital processing system operable to receive said digital signal from said analog to digital converter and generate at least one output signal within said frequency band (see column 25, lines 60-61 the ILS processing and column 23, lines 124-36, digital processing of ILS signals), said digital processing system comprising: a digital down converter operable to select said at least one frequency with said frequency band (see Fig. 3A, element DDC 210, and see frequency translation tuning performed by the DDC, column 26, lines 29-32); and a digital signal processor coupled to said digital down converter (Fig. 3A, DSP 216 and DDC 210 are coupled), said digital signal processor operable to extract information from said at least one of frequencies and generate at least one output signal (see column 10, lines 49-67, column 11, lines 1-7 see for example message processing and/or low-data rate speech algorithms performed by the DSP).

Phillips et. al. do not expressly teach: analog signal simultaneously carrying a plurality of channels within said frequency band; a single digital signal simultaneously carrying said plurality of channels within said frequency band.

In the same field of endeavor, Caldwell disclose: an analog signal simultaneously carrying a plurality of channels within said frequency band (Fig. 5A, Fig. 5B, column 4, lines 44-47, analog receiver receives (analog) RF signals, see column 8, through column 9, example 1 (or any other example)), simultaneously carrying said plurality of channels within said frequency band (see column 8, lines 53-58, all signals (these are channels) in the range)).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Phillips et. al. based on the teachings of Caldwell so that the analog signals received by Phillips et., al., simultaneously carry a plurality of channels within said frequency band, so that minimal components are used for CNST functions between 2 and 2000MHz (column 4, lines 59-67, column 5, lines 1-17). Based on the combination of teachings of Phillips and Caldwell, the digital signal of Phillips signal simultaneously carries said plurality of channels within said frequency band.

With respect to claim 44, claim 44 Phillips discloses: wherein said output signal comprises a time-domain multiplexed serial data link (see column 23,lines 34-37 and Fig. 6 where the signals are processed in a time-domain multiplex fashion and therefore the output of the digital processing system is also TDM).

With respect to claim 45, Phillips further discloses: further comprising means for generating a plurality of signals from said time-domain multiplexed serial data link for transmission to a plurality of end devices (Fig. 8B, serial interface 114 (UART), see column 12, lines 60-67, also column 7, lines 47-55, where the plurality of signals are the signals out of the serial interface (UART) transmitted to the various computer components as shown in Fig. 8B).

With respect to claim 46, claim 46 is rejected based on a rationale similar to the one used to reject claim 29 above.

With respect to claims 47-49 (see Table 1 of Phillips et. al., where the specific types or aviation signals are listed, and see column 2, lines 45-56)

With respect to claims 50-52, these claims are rejected based on a rationale similar to the one used to reject claims 2-4 respectively.

With respect to claims 53-4, claim 53-4 are rejected based on a rationale similar to the one used to reject claim 49 above (with respect to the plurality of output signals, these are the plurality of output signals generated over time by DSP).

With respect to claim 57, claim 57 is rejected based on rationale similar to the one used to reject apparatus claim 53 above (assuming one front-end circuit group that comprises a plurality of front-end circuits)).

With respect to claim 58, Phillips further discloses: further comprising mixing said received radio signals to an intermediate frequency band (column 8, lines 36-38, where IF conversion injvolves mixing the received rf signals so that they are downconverted to IF).

With respect to claim 59, claim 59 is rejected based on a rationale similar to the one used to reject claims 11-12 and 14-15.

12. Claims 60, 18-24, 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et. al. (U.S. 5,859,878) in view of Caldwell et. al., (U.S.5,548 839) and in view of Analog Devices AD6624A data sheet 2002 (hereinafter referred to as the Analog Devices document).

With respect to claim 60, neither Phillips et. al., nor Caldwell expressly teach: wherein said digital processing system is operable to receive said digital signal and simultaneously generate more than one output signals corresponding to more than one of said plurality of channels within said frequency band.

In the same field of endeavor, the Analog Devices document discloses: digital processing system is operable to receive said digital signal and simultaneously

generate more than one out signals corresponding to more than one of said plurality of channels within said frequency band (page 14, input data ports section on left column, and schematic on front page where four tuner channels are shown see also product description section on the front page, see digitization of entire spectrum (frequency band) of carriers (channels) and selection of carriers (channels)).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Phillips et. al., because it eliminates redundant radios in wireless applications and allows for easy reconfiguration and a variety of applications (see front page of AD6624 spec sheet).

With respect to claim 18, claim 18 see above rejection of claim 34, and claim 18 is rejected based on a rationale similar to the one used to reject claim 60 above.

With respect to claims 19, 21-23, 26-27 see above rejection of claims 18, 5-7, 11-12, 14-15,

With respect to claim 28, Phillips et. al., disclose: a plurality of front-end circuit groups and a plurality of corresponding analog to digital converters, wherein said digital processing system is operable to receive a plurality of digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits of at least one of said front-end circuit groups (see Fig. 2, two AIU circuits (column 8, lines

45-49), antenna front-end circuits, and 2 ADC of Fig. 3, with respect to the generation of at least one output signal corresponding to a channel see above rejection of claim 18).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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SV
2/1/2008

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER